WHAT IS CLAIMED IS:

1. An image processing circuit driven by a clock signal for processing data expressed by a plurality of bits, comprising:

a level determining section for determining whether or not a value of input data is smaller than a preset value; and

a clock control section for supplying a clock signal that makes a bit corresponding to the preset value active, when said level determining section determines that the value of the input data is not smaller than the preset value and interrupting supply of a clock signal that makes a bit corresponding to the preset value active, when said level determining section determines that the value of the input data is smaller than the preset value.

2. The image processing circuit according to claim 1, wherein said level determining section delays the result of determination by preset delay time from when values of successively input data items are changed from a value which is not smaller than the preset value to a value which is smaller than the preset value until the preset delay time has elapsed in a case where the values of the successively input data items are changed from the value which is not smaller than the preset value to the value which is smaller than the preset value.

3. The image processing circuit according to claim 2, wherein the delay time is image processing time from when data is input to the image processing circuit until the data is output therefrom.

4. The image processing circuit according to claim 1, wherein said level determining section compares a value of input data with threshold values which are respectively set for a plurality of clock signals that make the bits active, and determines whether or not the value of the input data is smaller than the threshold values, and said clock control section divides a reference clock signal into a plurality of clock signals that make the bits active, supplies the clock signal corresponding to the threshold value if the value of the input data is not smaller than the threshold value and interrupts supply of the clock signal corresponding to the threshold value if the value of the input data is smaller than the threshold value based on the result of determination by said level determining section for comparing the value of the input data with the threshold values respectively set for the divided clock signals.

5. The image processing circuit according to claim 4, wherein said level determining section outputs an interruption signal for interrupting the clock signal corresponding to the threshold value when

the value of the input data is smaller than the threshold value, and said clock control section divides a reference clock signal into a plurality of clock signals that make the bits active, and interrupts supply of the clock signals according to an interruption signal from said level determining section.

6. The image processing circuit according to claim 5, wherein said level determining section outputs an interruption signal for the clock signal corresponding to the threshold value after delaying the interruption signal by preset delay time from when values of successively input data items are changed from a value which is not smaller than the threshold value to a value which is smaller than the threshold value until the preset delay time has elapsed in a case where the values of the successively input data items are changed from the value which is not smaller than the threshold value to the value which is smaller than the threshold value.

7. An image processing apparatus including an image processing circuit driven by a clock signal for processing image data expressed by a plurality of bits, comprising:

a level determining section for determining whether or not a density value of image data input to the image processing circuit is smaller than a preset

density value; and

a clock control section for supplying a clock signal that makes a bit corresponding to the preset density value active, when said level determining section determines that the density value of the input image data is not smaller than the preset density value and interrupting supply of a clock signal that makes a bit corresponding to the preset density value active, when said level determining section determines that the density value of the input image data is smaller than the preset density value.

8. The image processing apparatus according to claim 7, wherein said level determining section delays the result of determination by preset delay time from when density values of successively input image data items are changed from a value which is not smaller than the preset density value to a value which is smaller than the preset density value until the preset delay time has elapsed in a case where the density values of the successively input image data items are changed from the value which is not smaller than the preset density value to the value which is smaller than the preset density value.

9. The image processing apparatus according to claim 7, wherein said level determining section compares a density value of input image data with threshold values which are respectively set for

a plurality of clock signals that make the bits active, and determines whether or not the density value of the input image data is smaller than the threshold values, and said clock control section divides a reference clock signal into a plurality of clock signals used for the bits, supplies the clock signal corresponding to the threshold value if the density value of the input image data is not smaller than the threshold value and interrupts supply of the clock signal corresponding to the threshold value if the density value of the input image data is smaller than the threshold value based on the result of determination by said level determining section for comparing the density value of the input image data with the threshold values respectively set for the divided clock signals.

10. The image processing apparatus according to claim 9, wherein said level determining section outputs an interruption signal for interrupting the clock signal corresponding to the threshold value when the density value of the input image data is smaller than the threshold value, and said clock control section divides a reference clock signal into a plurality of clock signals that make the bits active, and interrupts supply of the clock signals according to an interruption signal from said level determining section.

11. The image processing apparatus according to

claim 10, wherein said level determining section outputs an interruption signal for the clock signal corresponding to the threshold value after delaying the interruption signal by preset delay time from when density values of successively input image data items are changed from a value which is not smaller than the threshold value to a value which is smaller than the threshold value until the preset delay time has elapsed in a case where the density values of the successively input image data items are changed from the value which is not smaller than the threshold value to the value which is smaller than the threshold value.

12. A control method for controlling an image processing circuit driven by a clock signal for processing data expressed by a plurality of bits, comprising:

a first step of determining whether or not a value of input data is smaller than a preset value; and

a second step of supplying a clock signal that makes a bit corresponding to the preset value active, when it is determined in said first step that the value of the input data is not smaller than the preset value and interrupting supply of a clock signal that make a bit corresponding to the preset value active, when it is determined in said first step that the value of the input data is smaller than the preset value.

13. The control method for the image processing

circuit according to claim 12, wherein said first step includes a step of delaying the result of determination by preset delay time from when values of successively input data items are changed from a value which is not smaller than the preset value to a value which is smaller than the preset value until the preset delay time has elapsed in a case where the values of the successively input data items are changed from the value which is not smaller than the preset value to the value which is smaller than the preset value.

14. The control method for the image processing circuit according to claim 12, wherein said first step includes a step of comparing a value of input data with threshold values which are respectively set for a plurality of clock signals that make the bits active, and determining whether or not the value of the input data is smaller than the threshold values, and said second step includes a step of dividing a reference clock signal into a plurality of clock signals that make the bits active, supplying the clock signal corresponding to the threshold value if the value of the input data is not smaller than the threshold value and interrupting supply of the clock signal corresponding to the threshold value if the value of the input data is smaller than the threshold value based on the result of determination in said first step of comparing the value of the input data with

the threshold values respectively set for the divided clock signals.

15. The control method for the image processing circuit according to claim 14, wherein said first step includes a step of outputting an interruption signal for interrupting the clock signal corresponding to the threshold value when the value of the input data is smaller than the threshold value, and said second step includes a step of dividing a reference clock signal into a plurality of clock signals that make the bits active, and interrupting supply of the clock signals according to the interruption signal.

16. The control method for the image processing circuit according to claim 15, wherein said first step includes a step of outputting an interruption signal for the clock signal corresponding to the threshold value after delaying the interruption signal by preset delay time from when values of successively input data items are changed from a value which is not smaller than the threshold value to a value which is smaller than the threshold value until the preset delay time has elapsed in a case where the values of the successively input data items are changed from the value which is not smaller than the threshold value to the value which is smaller than the threshold value.